REMARKS

Claims 1-21 are pending in this application, of which claims 1, 8, 12, and 17 are the independent claims.

Claims 8 and 12 have been amended.

I. ALLOWABLE SUBJECT MATTER

Applicants appreciate the Examiner's indication that claims 2-4, 7, 11, 13-16, and 18-21 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, as Applicants believe dependent claims 2-4, 7, 11, 13-16, and 18-21 to be dependent upon allowable independent claims (as will be explained below), Applicants have not rewritten claims 2-4, 7, 11, 13-16, and 18-21 in independent form at this time.

II. CLAIM REJECTIONS 35 U.S.C. § 102(e)

Claims 1, 5, 6, 8-10, 12, and 17 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,762,620 (hereinafter "Jang"). Applicants respectfully traverse this rejection.

A. Claims 1, 5, 6, and 17

Contrary to the Examiner's assertions, Jang does not appear to disclose the features of the present invention. Specifically, Jang does not appear to show "a second resistive element coupled to a second port" or "a second logic circuit coupled to the first logic circuit and the second resistive element" as recited in claim 1. Further, Jang does not appear to teach or show a second logic circuit that will interact with the first logic

circuit by "manipulating one or more of the plurality of binary termination signals," as also recited in independent claim 1.

The Examiner states in the second paragraph of Section 2 of the current Office Action that all claimed features of the present invention are taught in Jang in Col. 2, lines 10-67. Applicants respectfully disagree with the Examiner's characterization of Jang as this reference relates to the present invention.

The Examiner identifies "second resistive element (PM1 in FIG. 5)" (Office Action, Section 2, line 6). Element PM1, a PMOS transistor, is not "coupled to a second port" as recited in Applicants' claim 1 and asserted by the Examiner. Instead, Element PM1 is coupled between resistor RP1 and power supply VDD (Jang, Col. 6, line 66-67 and Col. 7, line 1), neither of which is alone a port as contemplated by the present invention. Applicants describe generally in the Specification at least at Paragraphs 0005-0010 that a port may be a chip pad included in a memory system or other similar apparatus. With specific reference to "a second port," Applicants describe at least at Paragraphs 0030-0033 that a variable output impedance may be provided to a port of a memory system. In contrast, the resistor and power supply of Jang are not connected to a memory system nor do they seem to have a variable output impedance provided thereon. See Jang, FIG. 5. As such, Jang does not appear to show "a second resistive element coupled to a second port."

The Examiner's description of Jang does not appear to show that the second logic circuit "is coupled to... the second resistive element," nor is it "adapted to modify a characteristic impedance of the second port by

manipulating one or more of the plurality of binary termination signals," as recited in Applicants' claim 1. Applicants have attempted to identify the elements of Jang as they relate to the present invention according to the current Office Action. Jang's element PM1, which the Examiner has described as a second resistive element, is a component of self-calibration unit 100. The Examiner has identified self-calibration unit 100 as the second logic circuit. Element PM1 is a working part of the self-calibration unit and has no function outside of this unit were it to be removed from the self-calibration unit and coupled to the self-calibration unit in place of the element currently coupled thereto (Jang's multiplexing unit). Thus, the supposed second logic circuit of Jang is not "coupled to… the second resistive element" as recited in Applicants' claim 1. As Applicants understand the Examiner's labeling and description of Jang as it relates to the present invention, the first resistive element of Jang is componentry of the pad termination circuit (not addressed by the Examiner), which receives control signals from the element the Examiner has described as a first logic circuit. The supposed first logic circuit of Jang is a multiplexer for selecting between inputs of the second logic circuit and a control signal generating unit (not discussed by the Examiner). The Examiner's description of Jang appears to show the second logic circuit transmits signals to and does not receive signals from the first logic circuit. Accordingly, the second logic circuit of Jang cannot "manipulat[e] one or more of the plurality of binary termination signals" generated by the first logic circuit as recited in claim 1.

As such, Jang does not appear to disclose the elements of the present invention as defined by independent claim 1. Accordingly, Applicants respectfully request the Examiner reconsider and withdraw this rejection.

Independent claim 17 recites similar features to those already discussed with respect to independent claim 1. For at least the same reasons as claim 1, claim 17 is allowable. Dependent claims 5 and 6 depend from patentable claim 1 and thus are allowable for at least the same reasons. Accordingly, Applicants respectfully request the Examiner reconsider and withdraw these rejections.

B. Claims 8-10 and 12

Applicants reiterate their traversal of the 35 U.S.C. § 102(e) rejection above. Applicants respectfully disagree with the Examiner's assertion that Jang teaches Applicants' invention as claimed in unamended claims 8 and 12. However, solely to expedite prosecution, Applicants have amended independent claims 8 and 12 to clarify that the method of providing multiple termination values uses a plurality of binary termination signals generated at a single source. These amendments were made only to make explicit what was implicit in the original claims and are not meant to limit the scope of the independent claims. No new matter has been added by these amendments.

Jang provides for "a first input for inputting a variable impedance value; a second input for inputting a fixed impedance value; and a selector for selecting one of the fixed impedance value and the variable impedance value". (Jang, Col. 2, lines 24-28) Here, as in FIG. 4, the system of Jang discloses separate inputs of impedance

values and a multiplexer that selectively outputs either a fixed impedance value or a variable impedance value based on a separate control signal. As discussed above with respect to independent claims 1 and 17, in the present invention binary termination signals are generated by a first logic circuit and *the same* binary termination signals may be manipulated by a second logic circuit. Jang does not appear to teach or show "modifying a characteristic impedance of a second port by manipulating one or more of the plurality of binary termination signals at a second logic circuit" as recited in amended independent claim 8. Jang cannot anticipate independent claim 8 because Jang does not appear to describe each and every element of the claim. Accordingly, Applicants respectfully request the Examiner reconsider and withdraw this rejection.

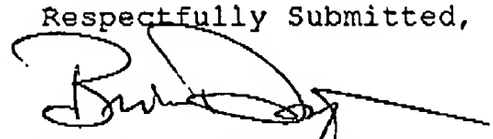
Independent claim 12 recites similar features to those already discussed with respect to independent claim 8. For at least the same reasons as claim 8, claim 12 is allowable. Dependent claims 9 and 10 depend from allowable claim 8 and thus are allowable for at least the same reasons. Accordingly, Applicants respectfully request the Examiner reconsider and withdraw these rejections.

III. CONCLUSION

The Applicants believe all the claims are now in condition for allowance, and respectfully request reconsideration and allowance of the same.

Applicants do not believe any Request for Extension of Time is required but if it is, please accept this paragraph as a Request for Extension of Time and authorization to charge the requisite extension fee to Deposit Account No. 04-1696. Applicants do not believe any other fees are due regarding this amendment. If any other fees are required, however, please charge Deposit Account No. 04-1696. The Applicants encourage the Examiner to telephone Applicants' attorney should any issues remain.

Respectfully Submitted,



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